

REMARKS

By the present amendment, claims 3 and 7 have been amended to obviate the examiner's objections thereto and/or to further clarify the concepts of the present invention. More particularly, claims 3 and 7 have been amended to add the phrase "by performing high density plasma chemical vapor deposition." This amendment is supported by the description on page 10, lines 9-20 of the subject specification. Entry of these amendments is respectfully requested.

In the Office Action, the drawings were objected to as not including the legend "Prior Art" with reference to Figure 1e. Accompanying this Amendment is a Letter re Drawings wherein it is requested that the legend be added to this Figure.

Claims 1-4 (it is believed that the rejection is directed to elected claims 3 and 4 only) were rejected under 35 USC § 102(e) as being anticipated by the patent to Zhang et al. In making this rejection, it was asserted that the cited patent teaches each step of the method as claimed. Reconsideration of this rejection in view of the above claim amendments and the following comments is respectfully requested.

As mentioned above, independent claim 3 has been amended herein to recite that insulation in the element partitioning trench and the mask aligning trench is performed by high density plasma chemical vapor deposition (HDP-CVD). It is submitted that the cited

patent to Zhang et al does not teach or suggest, among other things, performing HDP-CVD.

For the reasons stated above, withdrawal of the rejection under 35 U.S.C. § 102(e) and allowance of claims 3 and 4 over the cited Zhang et al patent are respectfully requested.

Claim 5 was been rejected under 35 USC § 103(a) as being unpatentable over the above patent to Zhang et al in view of the patent to Schoenfeld et al. In making this rejection, it apparently was acknowledged that the cited Zhang et al patent does not specifically teach the use of a rotary grinder in a CMP process, but has asserted that such is taught in the cited secondary patent in connection with a CMP process. Additionally, claim 6 was rejected under 35 USC § 103(a) as being unpatentable over the above patent to Zhang et al in view of the patent to Kuroi et al. In making this rejection, it apparently was acknowledged that the cited primary Zhang et al patent does not specifically teach (1) use of a silicon substrate, (2) having the insulation formed of silicon oxide and (3) forming a silicon oxide film beneath the silicon nitride film. The patent to Kuroi et al is alleged to supply these teaching deficiencies. Reconsideration of these rejections in view of the above claim amendments and the following comments is respectfully requested.

The above remarks relative to the teaching deficiencies of the Zhang et al patent are reiterated here with regard to this rejection of dependent claim 5. It is submitted that

the Schoenfeld et al patents do not supply the above-noted deficiencies.

Further, it is submitted that one of ordinary skill in the art would not employ the grinding as taught by the secondary Schoenfeld et al or Kuroi et al patent in the method as disclosed in the primary patent to Zhang et al. As is well settled, obviousness under Section 103 of the statute requires a teaching or suggestion in the art to combine the teachings of the patents as proposed with the expectation that the results achieved would have been predicted by that person of ordinary skill. It must be emphasized in support of the patentability of the subject invention over the teachings of the cited patents is that the patents provide no suggestion to motivate one of ordinary skill in the art to combine their teachings in the manner proposed by the examiner. It is well established principle of U.S. patent practice that the prior art must contain some suggestion for combination since without such, any combination is pure speculation on the part of the examiner and is based on a prohibited hindsight reconstruction from applicants' own disclosure. Accordingly, withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 5 and 6 over the cited patents are respectfully requested.

Claims 7 and 8 were rejected under 35 USC § 103(a) as being unpatentable over the above patent to Zhang et al in view of the patent to Kuroi et al. Similarly to the first rejection, the Zhang et al patent was applied as teaching the method as claimed, but it was acknowledged that the patent does not specifically teach (1) having the insulation formed of silicon oxide or (2) forming a silicon oxide film beneath the silicon nitride film or layer.

Reconsideration of this rejection in view of the above claim amendments and the following comments is respectfully requested.

As mentioned above, independent claim 7 has been amended herein to recite that insulation layers in the element partitioning trench and the mask aligning trench is performed by high density plasma chemical vapor deposition (HDP-CVD). It is submitted that the cited patent to Zhang et al does not teach or suggest, among other things, performing HDP-CVD. It is further submitted that this teaching deficiency is not supplied by the patent to Kuroi et al, among other things, the reasons set forth above.

For the reasons stated above, withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 7 and 8 over the cited Zhang et al and Kuroi et al patents are respectfully requested.

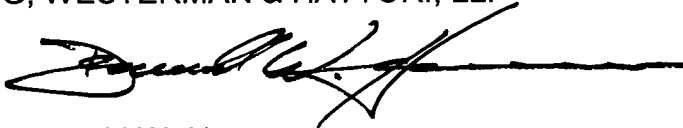
In view of the foregoing, it is submitted that the subject application is now in condition for allowance and early notice to that effect is earnestly solicited.

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In the event this paper is not timely filed, the undersigned hereby petitions for an appropriate extension of time. The fee for this extension may be charged to Deposit Account No. 01-2340, along with any other additional fees which may be required with respect to this paper.

Respectfully submitted,

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PATENT TRADEMARK OFFICE

Enclosure: Letter re Drawings

Marked Up Version of Amendments to Specification and Claims

IN THE CLAIMS:

Please amend claims 3 and 7 as follows:

3. (Amended) A method for manufacturing a semiconductor device, the method comprising:

forming an element partitioning trench and a mask aligning trench in a semiconductor substrate;

depositing an insulation in the element partitioning trench and the mask aligning trench by performing high density plasma chemical vapor deposition;

applying a protective mask on the insulation deposited in the element partitioning trench;

etching the insulation deposited in the mask aligning trench to remove some of the insulation; and

flattening an upper surface of the semiconductor substrate.

7. (Amended) A method for manufacturing a semiconductor device, the method comprising the steps of:

forming a silicon oxide film on an upper surface of a semiconductor substrate;

forming a silicon nitride film on the silicon oxide film;

partially removing the silicon nitride film and the silicon oxide film;

forming an element partitioning trench and a mask aligning trench by etching

the semiconductor substrate using a residue of the silicon nitride and silicon oxide films as a mask, wherein the element partitioning trench and the mask aligning trench have substantially the same depths;

simultaneously depositing a first layer of insulation and a second layer of insulation in the element partitioning trench and in the mask aligning trench, respectively, by performing high density plasma chemical vapor deposition;

coating the first insulation with a protective mask;

etching the second insulation so that a step is formed between an upper surface of the semiconductor substrate and an upper surface of the second insulation; and

removing the protective mask.